THAT WHICH IS CLAIMED IS:

1. An asynchronous frame receiver comprising:

an input for receiving asynchronous frames comprising standard characters, and a header comprising a break character with a data bit length greater than a data bit length of the standard characters;

a break character detection unit for detecting the break character; and

a standard character processing unit for detecting the standard characters, said standard character processing unit being activated by said break character detection unit based upon the break character being detected.

2. An asynchronous frame receiver according to Claim 1, further comprising a selection circuit for selecting a first operating mode in which said break character detection unit is deactivated, or a second operating mode in which said break character detection unit is active and controls said standard character processing unit.

3. An asynchronous frame receiver according to Claim 1, wherein said break character detection unit detects a break character formed of bits having a same value.

4. An asynchronous frame receiver according Claim 1, wherein the asynchronous frames comprise a synchronization character, and wherein said break character detection unit detects the synchronization character.

5. An asynchronous frame receiver according to Claim 4, further comprising a self-synchronization circuit for synchronizing a local clock signal of the receiver with a reference clock signal in the synchronization character.

6. An asynchronous frame receiver according to Claim 5, wherein said self-synchronization circuit is activated by said break character detection unit.

7. An asynchronous frame receiver according to Claim 1, wherein said break character detection unit comprises a first state machine, and wherein said standard character processing unit comprises a second state machine.

8. An asynchronous frame receiver according to Claim 2, wherein said selection circuit comprises a register for storing a mode bit.

9. An asynchronous frame receiver according to Claim 1, further comprising a substrate, and wherein said break character detection unit and said standard character processing unit are on said substrate so that the receiver comprises an integrated circuit.

10. A microcontroller comprising:

a universal asynchronous receiver transceiver (UART) comprising

an input for receiving asynchronous frames comprising standard characters, and a header comprising a break character with a data bit length greater than a data bit length of the standard characters,

a break character detection unit for detecting the break character, and

a standard character processing unit for detecting the standard characters, said standard character processing unit being activated by said break character detection unit based upon the break character being detected; and

a processor connected to said UART.

11. A microcontroller according to Claim 10, wherein said UART further comprises a selection circuit for selecting a first operating mode in which said break character detection unit is deactivated, or a second operating mode in which said break character detection unit is active and controls said standard character processing unit.

12. A microcontroller according to Claim 10, wherein said break character detection unit detects a break character formed of bits having a same value.

13. A microcontroller according Claim 10, wherein the asynchronous frames comprise a synchronization character, and wherein said break character detection unit detects the synchronization character.

14. A microcontroller according to Claim 13, wherein said UART further comprises a self-synchronization circuit for synchronizing a local clock signal of said UART receiver with a reference clock signal in the synchronization character.

15. A microcontroller according to Claim 14, wherein said self-synchronization circuit is activated by said break character detection unit.

16. A microcontroller according to Claim 10, wherein said break character detection unit comprises a first state machine, and wherein said standard character processing unit comprises a second state machine.

17. A microcontroller according to Claim 11, wherein said selection circuit comprises a register for storing a mode bit.

18. A method for processing asynchronous frames in an asynchronous frame receiver, the method comprising:

receiving as input by the asynchronous frame receiver the asynchronous frames comprising standard characters, and a header comprising a break character with a data bit length greater than a data bit length of the standard characters;

detecting the break character in the asynchronous frames using a break character detection unit; and

activating a standard character processing unit based upon the break character detection unit detecting the break character.

19. A method according to Claim 18, wherein the asynchronous frame receiver comprises a selection circuit for selecting a first operating mode in which the break character detection unit is deactivated, or a second operating mode in which the break character

detection unit is active and controls the standard character processing unit.

20. A method according to Claim 18, wherein the break character detection unit detects a break character formed of bits having a same value.

21. A method according Claim 18, wherein the asynchronous frames comprise a synchronization character, and wherein the break character detection unit detects the synchronization character.

22. A method according to Claim 21, wherein the asynchronous frame receiver further comprises a self-synchronization circuit for synchronizing a local clock signal of the asynchronous frame receiver with a reference clock signal in the synchronization character.

23. A method according to Claim 22, wherein the self-synchronization circuit is activated by the break character detection unit.

24. A method according to Claim 18, wherein the break character detection unit comprises a first state machine, and wherein the standard character processing unit comprises a second state machine.